REMARKS

In the Final Office Action mailed on January 9, 2006, the rejection of claims 1-16 was maintained. Applicant respectfully requests reconsideration of pending claims 1-16 in view of the following remarks.

I. Claim Objections

The Examiner has maintained the objections to claims 1 and 2. In maintaining the objections, the Examiner states, "if the die placements are different, the Examiner will like to suggest to applicant to change the claim language to show they are different." Applicant asserts that the Examiner is misreading the claims.

As an initial matter, Applicant notes that the Examiner objected to the use of "a die placement" in the preamble of claim 1 and in step a) of claim 1. In particular, the preamble of claim 1 recites that claim 1 is "a method of selecting a die placement." Step a) of claim 1 recites, "obtaining a die placement."

As set forth in MPEP 2111.02(II), preamble recitations can be mere statements of purpose or use. Applicant asserts that the statement "selecting a die placement" in the preamble of claim 1 is clearly a statement of purpose. Steps a) to d) recite the steps to achieve the stated purpose of selecting a die placement. Thus, it is logical to start the process of selecting a die placement by obtaining a die placement, which is **not necessarily** the die placement that will ultimately be selected by performing steps b) to d).

The Examiner also states, "the examiner is maintaining the claim objection as well as the position that there is only one die placement in the claims." Applicant asserts that this position is illogical in view of step d) in claim 1. In particular, step d) recites "adjusting the die placement to reduce the number of touchdowns." Thus, step d) requires that there be at least two die placements (i.e., the die placement before it was adjusted and the die placement after it is adjusted).

Finally, with regard to the Examiner's objection to the use of "a die placement" in claim 2, note that claim 2 recites iterating steps b) and d) of claim 1. Thus, step d) of "adjusting the die placement" is iterated, which results in multiple die placements being created. Claim 2 recites that steps b) and d) are iterated "to obtain a die placement with a minimum number of touchdowns." Note that the "die placement with a minimum number of touchdowns" may not exist until steps b) and d) are iterated. Thus, using the indefinite article is appropriate.

II. Claim Rejections – 35 USC 112

Claims 1-16 were rejected under 35 USC 112 as failing to comply with the written description requirement. The Examiner states that, "the specification does not clearly described [sic] that the dies are going to be fabricated as claimed."

Paragraph [0003] on page 1 of the present specification is reproduced below:

[0003] Semiconductor devices are typically manufactured by fabricating the devices on a semiconductor wafer. An individual device is formed as a die on the wafer using known semiconductor fabrication processes. Depending on the size of the die, a single wafer can contain hundreds of dies. **The dies are generally arranged in a pattern (i.e., a die placement) on the wafer** to maximize the number of dies on the wafer. (Emphasis added.)

Applicant asserts that it would be clear to one skilled in the art that the term "die placement" as used in paragraph [0003] refers to locations of the dies on the wafer. Also, paragraph [0004] on page 1 begins, "After the devices are fabricated on the wafer, the devices are electrically tested." Thus, it would be clear to one skilled in the art that the die placement referred to in paragraph [0003] defines the locations of the dies on the wafer before the dies are formed on the wafer.

The Examiner also states, "[i]t appears that the tester head defines the location on the wafer, which the dies are fabricated." Applicant asserts that this statement is illogical in view of what is well known in the art. In particular, as stated in paragraph [0004] on page 1 of the present

specification, it is well known that devices are electrically tested **after** they are fabricated on the wafer. Thus, it is illogical for the tester head to define locations on the wafer on which the dies are fabricated because the tester head would not be used until the dies have been fabricated.

III. Claim Rejections – 35 USC 103

Claims 1-16 were rejected under 35 USC 103(a) as being unpatentable over US Patent No. 6,640,423 (the Johnson reference) in view of admitted prior art.

Independent claims 1, 8, and 14 recite that the "die placement defines the locations on the wafer on which the dies are to be fabricated." In contrast, the Johnson reference relates to placement and bonding of a die on a substrate **after the die has been diced or cut from the wafer** on which it was formed. Thus, the "die placement" recited in claims 1, 8, and 14 is non-analogous to the placement of dies referred to in the Johnson reference.

As an initial matter, note that Applicant's assertion is **not** that the Johnson reference is nonanalogous art as suggested by the Examiner in the Final Office Action. Instead, as clearly stated above and in Applicant's earlier Response, Applicant's assertion is that **the "die placement"** recited in claims 1, 8, and 14 is **non-analogous to (i.e., not the same as)** the placement of dies referred to in the Johnson reference. Concluding from this assertion that Applicant's argument is that the Johnson reference is nonanalogous art mischaracterizes Applicant's assertion.

In the Final Office Action, the Examiner agrees that the Johnson reference does not disclose die placements that "define the locations on the wafer as claimed." The Examiner, however, asserts that, "the admitted prior art discloses that it is well known to use the die placement to define the location on the wafer, which the dies are to be fabricated." The Examiner cites to page 1, paragraphs [0003] and [0004] of the present specification.

Note that this assertion by the Examiner contradicts the Examiner's 112 rejection that, "[i]n viewing the specification, it is neither clear nor concise that the die placement defines the locations on the wafer." As set forth above, paragraphs [0003] and [0004] of the present

specification clearly states that the term "die placement" is being used to refer to locations on the wafer on which dies are to be fabricated, which the Examiner appears to rely on to substantiate the present 103 rejection.

The Examiner also asserts that "[i]t would have been well known and obvious to a person having ordinary skill in the art at the time the invention was made to have the die placement in Johnson et al. to define the location on the wafer since the prior art teaches that having the die placement to define the location on the wafer helps track the locations of the dies that fail or have low yield during test." Applicant asserts that the Examiner's assertion is illogical.

In particular, as repeated above, the placement of dies referred to in the Johnson reference are of dies **after they have been cut from the wafer**. In contrast, the testing referred to in paragraph [0004] of the present specification, which the Examiner appears to rely on to substantiate the present obviousness rejection, refers specifically to testing the dies **while the dies are still on the wafer**. Specifically, lines 3-4 of paragraph [0004] states, "[s]emiconductor manufacturers are increasingly performing comprehensive testing of dies, meaning that each die is tested, **while the dies are still on the wafer**." (Emphasis added.) Thus, the testing described in paragraph [0004] is incompatible with the testing disclosed in the Johnson reference because paragraph [0004] describes **testing dies that are still on the wafer** while the Johnson reference discloses **testing dies after they have been cut from the wafer**.

Additionally, in the Final Office Action, the Examiner continues to assert that probe 604 corresponds to the tester head recited in claim 1. Note that claims 1, 8, and 14 recite that the die placement is adjusted to reduce the number of touchdowns (the number of times the tester head is lowered) to test the dies in the die placement. However, as depicted in FIG. 47C and described in column 10, lines 50-67, the Johnson reference discloses that probe 604 is a component of an oscillation frequency detection assembly 600 that controls the amount of bump height compression of the die, the substrate, or both, during bonding. The Johnson reference does not disclose adjusting the die placement on die holder 100 to reduce the number of touchdowns made by probe 604.

Thus, Applicant asserts that claims 1, 8, and 14 are allowable over the Johnson reference. Additionally, Applicants assert that claims 2-7, 9-13, and 15, 16 are allowable for at least the reason that they depend from allowable independent claims.

IV. Conclusion

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue. If it is determined that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the event the U.S. Patent and Trademark office determines that an extension and/or other relief is required, Applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to Deposit Account No. 03-1952 referencing docket no. 524322001200. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

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Respectfully submitted,

By _____

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